Insulating Biomaterials N01-NS--2-2347

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Neural Prosthesis Program

InnerSea Technology

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Third Quarter Summary

The goal of the Insulating Biomaterials work is to identify and evaluate materials, coatings, and assembly techniques suitable for protection of integrated circuit devices being considered for neural prosthetic applications.

Long Term Soak Test Database

Keeping track of the various samples under long term testing in a safe and reliable way has long been an issue with this program. During the past three quarters, a data base structure has been developed to allow long term archiving of data for all our devices. Initially, this has been fully implemented for the long term soak system. All prior data has been transcribed into the new format and all new data is being acquired directly to the database. Programs for extracting information of interest from the database have been written and are in use in reviewing data periodically. After each sweep is completed for a measurement sequence, the database is copied to a central server for backup and to make the data available over the local area network.

Silicone Adhesion and Bonding

Additional testing targeted towards solving the issues of encapsulation of battery lead wires continued. A variety of cleaning and pre-treating methods were attempted to improve the adhesion with ambiguous results. However, it was determined that soaking the wire in water prior to bonding seemed to enhance bonding somewhat. Next quarter adhesion promoters will be studied. Peel testing of silicone on quartz and glass continued. Additional parameters of cure cycle, mixing, humidity, pre-treatments were evaluated. While results were still variable, variability was less and peel strengths were limited to the strength of the material under test in general. However, the strength of the materials under test was quite variable. The variability in strength does not seem to be related to any processing parameters studied thus far, and thus must in some way be due to an unrelated phenomenon. Adhesion promoters may be of some value here in stabilizing the bonding surface.

PassTest Integrator

A system design was developed to provide overall guidance for the test system, and is appended. This is a preliminary design which is being considered and will be modified as needed to result in an efficient, relatively low cost per channel measurement system that is easily maintained and used.

CVD Synthesis of New Materials

An investigation of the origin of the defects in the silicone Hot Filament Chemical Vapor Deposition (HFCVD) films continued. Films fabricated with nichrome filament wires had incorporated metals which were apparently responsible for formation of pores and inclusions that compromised film performance. Alternate filament materials were investigated and it was found that elimination of metal contamination resulted in reduced film defects. Film growth rates were relatively slow, however, because the catalytic properties of the new filament materials were not sufficient for high growth rates. Increasing the temperature of the filament did increase film growth rates, but resulted in more brittle films due to the higher deposition temperatures. An alternate reactant chemistry will be explored to hopefully identify a vapor phase catalyst that will promote rapid film growth at low filament temperatures.

Passivation Test System 030515

System Architecture

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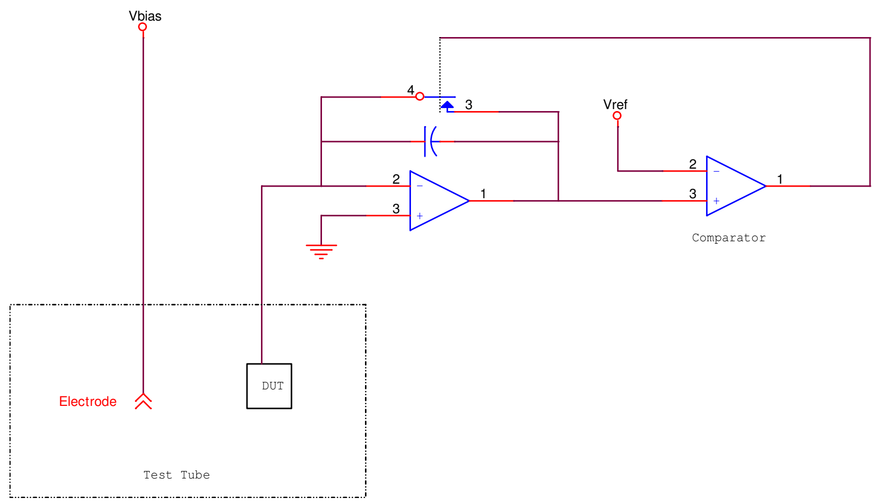
Purpose

This document will outline the architecture of the new Passivation Test System – Model 0305015 Revision A

Overview

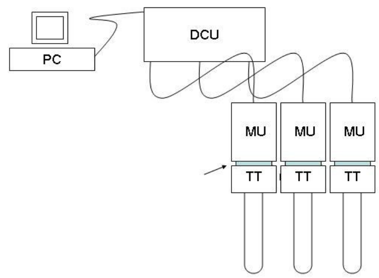
The Model 030515 Passivation Test System performs high sensitivity leakage measurements on many samples simultaneously. The measurements are performed using integrators that accumulate the leakage current over time until a fixed threshold level is reached. The amount of time it takes a particular device to reach this threshold level can then be used to calculate the average leakage during the test period, and knowing the bias voltage level used to force the leakage, calculate the resistance of the device. The results of the test can then be read out, and archived using a host PC. The integrator is then reset to begin the next measurement. The basic circuit appears below:



Details

The system consists of 4 major parts:

1) The tube top PCB which has solder pads for attaching the DUT connections, and an EEPROM to store the device name, serial number, and optionally a short description.
2) The measurement unit, (MUs), attaches directly to the tube top PCB, and contains all of the analog circuitry for performing the measurement, and continuity testing of the device. In addition, another EEPROM device is present to hold the unit's serial number, its associated calibration data, and the value of each device's self test resistor.
3) The data collection/processing unit, (DCU), connects to several (16 at this writing) MUs. The DCU times the period between device resets, calculates the current, and resistances based on the stored calibration data on the MU. The DCU also handles communication with the host PC, self-test functionality, Vbias setup, and continuity test.
4) The host PC which serves as the user interface and the data archive for the system. This PC runs software specifically designed to interface to the DCU via the USB port. Several DCUs can be connected to the host PC, using a USB hub. Data and jar information are stored in an ODBC compliant database product.



Operation

On system startup the PC will instruct the DCU to download the data from the EEPROMS on the tube top PCBs. The jar data will be sent to the host PC, where it will be correlated with the existing device table. If the information does not correlate, such as when a new device is added to the system or an old device is removed, then the user will be presented with a list of options to correct the local table. Once the data correlates, the PC will instruct the DCU to download the data from the EEPROMS on the MUs. This information will be sent to the host PC to be correlated with the MU table. Again, any problem with the correlation will result in a request for user intervention. These two steps allow us to always know which jar is paired with which MU, and where each jar is located. Once correlated, the host PC will instruct the DCU to download the MU calibration data to its local table for use in making the current and resistance calculations. Next the host PC will instruct the DCU to begin its self test procedure. The DCU begins by instructing the MUs to disconnect the DUT, and connect its self test resistor to the measurement circuit. The DCU will then set up the Vbias level for the system, and issues a system wide integrator reset. The measurement then commences for all of the MUs. Once all measurements are complete, the DCU calculates the current, and resistance of each test resistor, and compares this value to the one stored in the EEPROM. Any deviation from this value of more than 1% generates a request for user intervention, flagging the MU as out of tolerance. If the tests pass, then the host PC will request the DCU to connect the DUTs to the system and begin continuity testing on all devices. The results of this test are presented to the host PC as pass/fail, and are again correlated with the existing device table since not all devices will be set up for continuity tests. Any failures will be noted in the device table, but testing will not stop. Once the continuity testing is completed, the host PC instructs the DCU to begin normal testing. The tests proceed as follows:

1) The DCU sets the Vbias level for all devices on the system. Each jar has an 8 bit serial D/A unit associated with it so that different voltage levels can be used for different devices. The Vbias is buffered on each MU, and is connected to the DUT through a series resistor, 4 per MU. The voltage on the DUT side of the resistor is fed back to the DCU, and used for the calculations. We can also detect a shorted unit with this feature.
2) The DCU issues a system wide integrator reset. This begins the test with the integrators starting at a known level. This only occurs during the self test and on the first test after startup.
3) The integrators begin running.
4) When an integrator output reaches the Vref level, a reset strobe is sent to the device's associated one-shot, and also to the DCU. The one-shot insures the integrator is reset consistently.
5) When the DCU receives the reset signal form a device, the associated 32 bit counter's value is dumped to a register. The counter is then reset, and restarted.
6) The DCU reads the counter register value, and calculates the current, and resistance. The results are stored in local registers.
7) The host PC reads the DCU registers at timed intervals, and records the data in the database archive.

Architecture

Tube Top PCB

The only active device on the tube top PCB is the serial EEPROM which holds identifying information regarding the device it is attached to. All of the device connections are passed directly to the MU. Serial EEPROMS are a very low cost component, and it is preferable to attach the device mechanically to the jar, for future reference if necessary. The signal map is as follows:

DEV4IN	Input	Device 1 Input
DEV4COUT1	Output	Device 1 Continuity Output 1
DEV6IN	Input	Device 2 Input
DEV6COUT1	Output	Device 2 Continuity Output 1
DEV8IN	Input	Device 3 Input
DEV8COUT1	Output	Device 3 Continuity Output 1
DEV10IN	Input	Device 4 Input
DEV10COUT1	Output	Device 4 Continuity Output 1
DEV4RET	Input	Device 1 Return
DEV4COUT2	Output	Device 1 Continuity Output 2
DEV6RET	Input	Device 2 Return
DEV6COUT2	Output	Device 2 Continuity Output 2
DEV8RET	Input	Device 3 Return
DEV8COUT2	Output	Device 3 Continuity Output 2
DEV10RET	Input	Device 4 Return
DEV10COUT2	Output	Device 4 Continuity Output 2
REFELECT	Input	Reference Electrode
SCLK	Input	Serial EEPROM Clock
SDATA	Output	Serial EEPROM Data
SCS	Input	Serial EEPROM Chip Select
VCC	Power	Serial EEPROM Power
GND	Power	Serial EEPROM Ground

Measurement Unit (MU)

The measurement unit contains all of the analog circuitry necessary to make the leakage measurement. In addition, the integrator reset, serial EEPROM, Vbias buffer, continuity, and self test circuitry also reside here. The MU is independent of the tube top, allowing the unit to be moved to a new jar after the old jar has been terminated. The MU is a compact, sophisticated, and potentially expensive unit, so we do not want to have to condemn it along with the tube it is testing. The signal map is as follows:

+15V	Power	
-15V	Power	
GND	Power	
GLOBALRST#	Input	Global Reset from DCU
DECRST4#	Output	Device #1 Reset
DECRST6#	Output	Device #2 Reset
DECRST8#	Output	Device #3 Reset
DECRST10#	Output	Device #4 Reset
SELFTEST	Input	Signal to switch to Self Test mode
SCLK	Input	Serial EEPROM Clock
SDATA	Output	Serial EEPROM Data
SCS0	Input	Serial EEPROM Chip Select
SCS1	Input	Serial EEPROM Chip Select
BIASRET4	Output	Vbias Return Device # 1
BIASRET6	Output	Vbias Return Device # 2
BIASRET8	Output	Vbias Return Device # 3
BIASRET10	Output	Vbias Return Device # 4

Vbias	Input	Device Bias Voltage
CONTINUITY	Input	Switch to Continuity Test mode

Data Collection/Processing Unit (DCU)

The DCU is the most sophisticated portion of the entire system. The DCU integrates the counters and control logic, the USB controller, a PIC18F458 microcontroller, status display, local program and data memory, and power supplies, in a single unit. The counters and control logic are controlled by multiple Altera ACEX 1K PLD devices which are in system programmable for future upgrades or bug fixes. The PIC18F458 is also an ISP compatible, for program upload and debug. The USB communications is controlled by a FT245BM integrated USB controller chip. 16 jars can be handled by a single DCU, and additional DCUs can be connected to a single host PC through a USB hub.

The PIC acts as the command interpreter for data received over the USB link. It also loads calibration, and device data in local registers for use in making leakage current, and device resistance calculations. The PIC also controls the power-on-reset functionality of the DCU, and is connected to each of the supported devices.

The Altera ACEX 1K PLD is in a fashion more similar to FPGA devices in that it does not store its configuration data on board. An external configuration device, the EPC16, stores the configuration, and uploads it upon POS. The EPC16 is programmable via the JTAG port for ISP. The Altera devices contain 32-32 bit counters with their associated control circuitry. Additionally, the address decoding, and data routing for the MU and Tube Top PCB EEPROMS are performed by these devices.

Host PC

The Host PC controls the DCU via an USB link. The Host PC maintains a database of collected data, and initiates startup and self-test procedures for the system. The Host PC programming will be in Visual Basic, with hooks to an ODBC compliant database product. One of the most important features of the Host PC is to maintain a strict correlation between the installed test devices, their associated MU, and the local record of the current setup. Any discrepancy between these items will immediately flag the operator. Jar setup as it is with the old system will go away, in favor of a “plug-and-play” style of operation. Jars will be recognized by the system, and their basic descriptors, location, and MU. The user will only need to confirm the addition/subtraction of a device, and add comments. Since the measurement process is no longer keyed to a specific location, any jar can be moved anywhere, without having to make changes to the setups.